DataSheet

CN121

3mm × 3mm QFN16, Medical Level, Low-Power Single-Lead ECG AFE

1 Features

- √ Fully integrated one chip solution, few external components
- √ 70 µA operating current, extremely low power consumption
- √ Optional third RLD electrode
- √ Integrated filter with programmable bandwidth, fit for various application recipes
- √ YY0885 / YY9706-2-47 / IEC60601-2-47 compatible
- √ <100 ms fast restore time
- √ DC lead-off detection with adjustable environment disturbance immunity
- √ 1.8 V core power supply, 1.8 V/3.3 V digital IO power supply
- √ Flexible sensing/standby/powerdown power mode
- √ Baseline wandering removal at analog-end
- √ 105 dB CMRR (typical case)
- √ Single-end analog output
- √ ±8 kV HBM ESD rating

2 Applications

Wearable Devices

- Smart watches/wristbands
- Smart health clothes
- ECG monitoring straps
- Remote health monitoring cards

Health Monitoring Scenes

- Fitness equipment
- Bicycles
- Smart cars

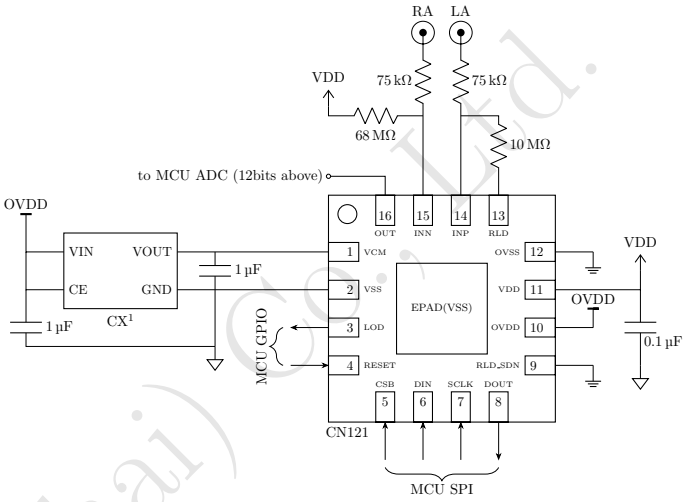

Figure 1: Application highlight

3 Description

The CN121 is a fully integrated one chip solution for electrocardiogram (ECG) or similar biopotential acquisition applications. It is designed to amplify and filter weak ECG signals in the presence of noisy or undesirable environment, such as large power-line interference or motion/electrode placement effect. An embedded microcontroller with 12bits ADC can be adopted easily to further acquire and process the single-end analog output signal.

Due to its large input impedance, high common-mode rejection ratio (CMRR) even without the third RLD electrode, and large DC input unbalance voltage tolerance, single lead ECG with two Dry electrodes is supported with excellent waveform quality.

An SPI interface is used to write and read the config registers of the CN121, including the clinical-level bandwidth selection, and the 16-grade programmable gain. It is easy to be programed by the most common MCU.

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Low-Power Single-Lead ECG AFE

Contents

4 Revision History

12/2023–Rev.2.0: New Version
07/2024–Rev.2.1: Update something
04/2026–Rev.3.0: Update application circuit, detailed description & features

5 Pin Configuration and Functions

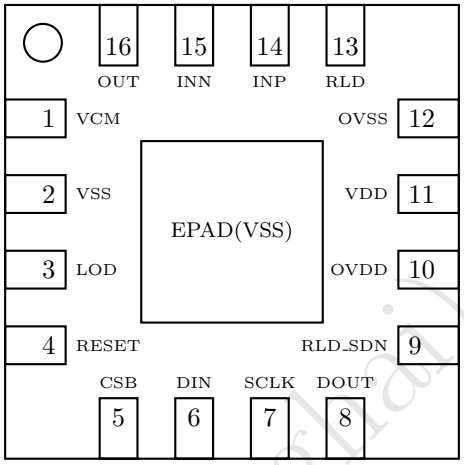


Figure 2: QFN16 pin configuration

Table 1: QFN16 pin function description

Number	Name	Function	Description
1	VCM	Analog Input	Common Mode Voltage Input, connects to a midsupply reference.
2	VSS	Supply	Core Supply Ground.
3	LOD	Digital Output	Lead Off Detection Output, active high, indicates the lead off state.
4	RESET	Digital Input	Reset Input, active high, resets the config registers and SPI state.
5	CSB	Digital Input	Chip-Select Input, active low, enables the SPI transfer.
6	DIN	Digital Input	Serial Data Input, sampled into the device on the falling edge of SCLK.
7	SCLK	Digital Input	Serial Clock Input, clocks data in and out of the SPI.
8	DOUT	Digital Output	Serial Data Output, changes state on the rising edge of SCLK.
9	RLD_SDN	Digital Input	Right Leg Drive Shutdown Control Input, active high, shutdown the RLD functionality.
10	OVDD	Supply	IO Supply Power, 1.8 V/3.3 V.
11	VDD	Supply	Core Supply Power, 1.8 V.
12	OVSS	Supply	IO Supply Ground.
13	RLD	Analog Output	Right Leg Drive Output, connects to the driven electrode if the RLD functionality is used.
14	INP	Analog Input	Positive ECG Channel Input, connects to the input electrode.
15	INN	Analog Input	Negative ECG Channel Input, connects to the input electrode.

Table 1: QFN16 pin function description (continued)

16	OUT	Analog Output	ECG Channel Output, single-ended.
EPAD	VSS	Supply	Exposed Pad, connects to the core supply ground.

6 Specifications

6.1 Absolute Maximum Ratings

Table 2: Absolute maximum ratings

	Min	Max	Unit
VDD to VSS	−0.1	1.9	V
OVDD to VSS	−0.3	3.6	V
Analog input to VSS	−0.1	the lower of (1.9 and VDD + 0.1)	V
Digital input to VSS	−0.3	the lower of (3.6 and OVDD + 0.3)	V
Input current to any pin except supply pins		±10	mA

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

6.2 ESD Ratings

Table 3: ESD ratings

		Value	Unit
Electrostatic discharge	Human Body Model (HBM), per ESDA/JEDEC JS-001-2017, all pins	±8	kV
	Charged Device Model (CDM), per ESDA/JEDEC JS-002-2018, all pins	±1	kV

6.3 Electrical Characteristics

Table 4: Electrical characteristics

specifications are at V_{VDD} = 1.8 V, voltage at VCM pin (V_{VCM}) = V_{VDD}/2, R_{VCM} = 100 kΩ, C_{VCM} = 10 µF and G_{CH} = 480, only characterized at 25 °C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ECG CHANNEL						
AC Differential Input Range	$V_{in,AC}$	$V_{in,DC}$ = 0 V, $V_{in,CM}$ = 0 V, THD <0.3% , G_{CH} = 60		±10		mV_{pp}
DC Differential Input Range	$V_{in,DC}$	$V_{in,AC}$ = 2 mV_{pp}, $V_{in,CM}$ = 0 V, THD <0.3%		±500		mV
Common Mode Input Range	$V_{in,CM}$	from V_{VCM}, $V_{in,DC}$ = 0 V, $V_{in,AC}$ = 0 V, THD <0.3%		±1.2		V_{pp}

Table 4: Electrical characteristics (continued)

specifications are at V_{VDD} = 1.8 V, voltage at VCM pin (V_{VCM}) = V_{VDD}/2, R_{VCM} = 100 kΩ, C_{VCM} = 10 µF and G_{CH} = 480, only characterized at 25 °C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Mode Rejection Ratio	CMRR	0 Ω source impedance, $f_{in,CM}$ = 50 Hz, $V_{in,AC}$ = 0 V, $V_{in,DC}$ = 0 V, $V_{in,CM}$ = 600 mV_{pp}, BW = 4-40Hz	95	105		dB
Input Refered Noise	V_n	BW = 4-40Hz		1.4		μV_{rms}
		BW = 0.05-300Hz		2.6		
Input Impedance	Z_{in}	Differential		40||8		GΩ||pF
		Common Mode		20||16		
Total Harmonic Distortion	THD	$V_{in,AC}$ = ±10 mV_{pp}, f_{in} = 10 Hz, $V_{in,DC}$ = 0 V, $V_{in,CM}$ = 0 V, G_{CH} = 60			0.3	%
Gain Settings	G_{CH}	programmable		60 to 960		
High-pass Cutoff Frequency	f_{HP}	programmable		0.05, 4		Hz
Low-pass Cutoff Frequency	f_{LP}	programmable		40, 55, 150, 300		Hz
Channel Gain Error	G_{err}	$V_{in,AC}$ = ±2 mV_{pp}, f_{in} = 10 Hz,BW = 0.05-300Hz	−10		+10	%
Fast Settling Restore Time	T_{rec}			100		ms
Power Supply Rejection Ratio	PSRR	f_{PS}=50Hz		82		dB
Maximum Output Loading Capacitance	C_{load}			600		pF
LEAD OFF DETECTION (LOD)						
Comparing Threshold Voltage	$V_{th,LOD}$			1.5		V
Hysteresis	$V_{hyst,LOD}$			125		mV
DIGITAL INPUT/OUTPUT						
Input Voltage High	V_{IH}	V_{OVDD} = 1.8 V		1.5		V
		V_{OVDD} = 3.3 V		3.0		
Input Voltage Low	V_{IL}	V_{OVDD} = 1.8 V		0.3		V
		V_{OVDD} = 3.3 V		0.3		
Output Voltage High	V_{OH}	V_{OVDD} = 1.8 V		1.8		V
		V_{OVDD} = 3.3 V		3.3		
Output Voltage Low	V_{OL}	V_{OVDD} = 1.8 V		0		V
		V_{OVDD} = 3.3 V		0		
SYSTEM SPECIFICATIONS						
Core Supply Range	V_{VDD}		1.7	1.8	1.9	V
IO Supply Range	V_{OVDD}		1.7	1.8	3.6	V

Table 4: Electrical characteristics (continued)

specifications are at V_{VDD} = 1.8 V, voltage at VCM pin (V_{VCM}) = V_{VDD}/2, R_{VCM} = 100 kΩ, C_{VCM} = 10 µF and G_{CH} = 480, only characterized at 25 °C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Core Supply Current	$I_{supply,VDD}$	Sensing Mode, RLD_SDN = low		80		µA
		Sensing Mode, RLD_SDN = high		70		
		Standby Mode		7		
		Shutdown Mode		0.5		
IO Supply Current	$I_{supply,OVDD}$				1	µA
TEMPERATURE						
Operating temperature range			0		+70	°C

6.4 Timing Characteristics

Table 5: Timing characteristics

specified at 25 °C; load on D_{OUT} = 20 pF ‖ 100 kΩ; V_{VDD} = 1.8 V, V_{OVDD} = 1.8 V

Symbol	Description	Min	Nom	Max	Unit
t_{SCLK}	SCLK period	50			ns
t_{CSSC}	CSB low to first SCLK, setup time	6			ns
$t_{SPWH,L}$	SCLK pulse width, high and low	15			ns
t_{DIST}	DIN valid to SCLK falling edge: setup time	10			ns
t_{DIHD}	Valid DIN after SCLK falling edge: hold time	10			ns
t_{DOPD}	SCLK rising edge to DOUT valid			12	ns
t_{CSH}	CSB high pulse	2			ns
t_{CSDOD}	CSB low to DOUT driven	10			ns
t_{SCCS}	Eighth SCLK falling edge to CSB high	3			ns
$t_{SDECODE}$	Command decode time	4			ns
t_{CSDOZ}	CSB high to DOUT Hi-Z			10	ns

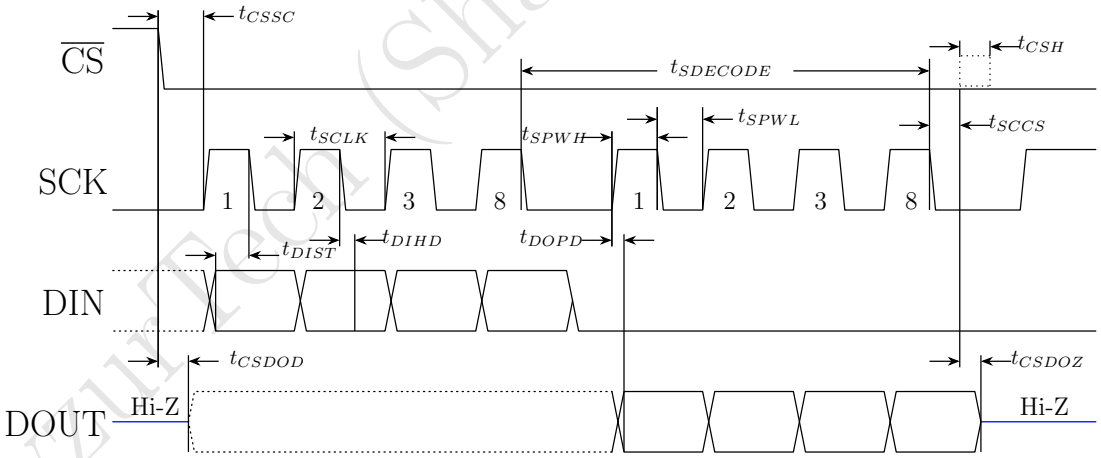


Figure 3: Serial Interface Timing

7 Detailed Description

7.1 Overview

The CN121 is a fully integrated front end for signal conditioning of cardiac (ECG) or other biopotentials (sEMG, EEG, etc.).
It consists of a specialized biopotential acquisition channel, DC leads on or off detection functionality and optional right leg drive circuitry.

7.2 Biopotential Acquisition Channel

The biopotential acquisition channel is the most important part of the analog frontend, which determines the quality of the biopotential signal acquired. The CN121 contains a specialized amplification channel developed by CyzurTech®, including Radio Frequency Interference (RFI) filters, an elegantly designed instrumentation amplifier (IA), programmable gain amplifier (PGA), etc.
The >95 dB (worst case) common mode rejection ratio ensures that it can withstand large common mode interference such as power-line disturbance in annoying environments.
The baseline wandering is largely removed at analog-end and the input noise level is low enough, enabling a clinical level waveform quality.
The integrated bandpass filter owns a programmble bandwidth which can be used for various application recipes(for example, the 0.05Hz high-pass pole to ensure the clinical bandwidth of 0.67Hz-40Hz, the 4Hz high-pass pole to fit sports related application).
The power consumption is maintained at 70 µA per channel, and dry electrodes are supported due to its high input impedance (>20 GΩ) and large DC input unbalance voltage tolerance (±500 mV).

7.2.1 RFI Filter

Radio frequency (RF) rectification is often a problem in applications where there are large RF signals. The CN121 has a low-pass filter on each input, suppressing signals with frequency higher than 1 MHz.
It is **strongly adviced** to connect a 75 kΩ or 100 kΩ at each input in series for best RFI effect at low-frequency (<40 Hz).

7.2.2 Programmable Gain

A 16-grade programmable gain setting is provided through the SPI interface. The base gain factor is 60 and the ratios are 2's multiples.
Larger gains will scale the ECG signal to a more detailed extent, suppressing the MCU ADC noise effect on channel inputs while more sensitive to the power-line disturbance (the signal at the analog output more easily saturated).
It is advised to select the 120x or 240x gain for cardiac applications, according to the power-line environment condition or different lead setups.

7.2.3 Fast Restore Circuit

Because of the low cutoff frequency used in the integrated high-pass filter, signals may require several seconds to settle. This settling time can result in a delay for the user after a step response, such as when the electrodes are first connected. This fast restore function is implemented internally, and the ECG channel can restore from the abnormal states and resettle to its ideal operating points in 100 ms time.
It is like an analog reset and the user must deassert it again to sense the ECG signal continuously.
It is controled by the SPI interface and see the SPI interface section to know more details.

7.2.4 Common-Mode Voltage

The CN121 needs a customized CX chip to create a mid-supply common-mode voltage, driving the VCM pin which does not own a buffer inside.
The output voltage and the internal reference voltage of the ECG Channel are referenced around this voltage.

7.3 Right Leg Drive (RLD) Circuitry

The RLD circuitry is used to drive a third electrode attached to the body. For the CN121, it is optional and has two main purposes: a) drive the body to a proper midsupply DC voltage so the ECG channel can work right; b) lower the common-mode interferece on the body, thus improving the common-mode rejection of the system.
Due to the intrinsic high CMRR of the ECG channel, this RLD circuitry does not employ the common feedback & subjection design concept. RLDFB feedback pin is saved and the feedback capacitor or resistor in the loop is not needed.

7.4 DC Leads Off Detection (LOD)

The DC leads off detection mode can be used in two or three electrode configurations.
This mode works by sensing when either instrumentation amplifier input voltage is within 0.2 V from the positive rail.
If there is large power-line interference at the environment, the LOD signal may became a 50/60Hz pulse wave with certain duty ratio in accordance with the power-line interference severity. Users must handle the duty ratio detection by software or hardware (more power-saving).

7.5 Power Mode

The CN121 has three power modes: Sensing Mode, Shut-down Mode, and Standby Mode. They can be programmed through the SPI interface.
In sensing mode, the ECG channel and the LOD circuitry keeps detecting whether lead is off.
In shut-down mode, all the analog blocks are off, the power consumption reaches the lowest level.
In standby mode, the LOD circuitry keeps detecting whether lead is on, while the ECG channel is off. This is specially useful for some portable applications where low power consumption is critical. It only consumes 7 µA in standby mode. The microcontroller enters sleep mode when the electrodes are disconnected, and the LOD signal acts as an interrupt to wake up the microcontroller.
For all the three power mode, the SPI interface is on.

7.6 SPI Interface

The SPI-compatible serial interface consists of four signals: CSB, SCLK, DIN and DOUT. The interface reads and writes registers, thus controlling CN121 operation. There are two commands supported, RREG and WREG, which stand for reading registers and writing registers, separately. They are both multi-byte commands and the SPI transfer must follow a strict format in order to succeed.

7.6.1 Chip Select (CSB)

CSB selects the CN121 for SPI communication. CSB must remain low for the entire duration of the serial communication. When CSB is taken high, SCLK and DIN are ignored, and DOUT enters a high-impedance state.

7.6.2 Serial Clock (SCLK)

SCLK is the SPI serial clock. SCLK is used to shift commands in shift data out from the device. The serial clock features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the CN121. Even though the input has hysteresis, it is recommanded to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device, as required by the command format. The timing between SCLK pulses can be loose, but the transfer will strictly follow the command format. If the interface going to an unknown state, take RESET high to reset the transfer state and the internal registers.

7.6.3 Data Input (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the CN121 (opcode commands and register data). The device latches data on DIN on the SCLK falling edge.

7.6.4 Data Output (DOUT)

The data output pin (DOUT) is used with SCLK to read register data from the CN121. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when CSB is high.

7.6.5 RREG: Read Registers

The RREG command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read – 1.
First opcode byte: 001r rrrr, where r rrrr is the starting register address.
Second opcode byte: 000n nnnn, where n nnnn is the number of registers to read – 1.
The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 4. The RREG command can be issued at any time.

7.6.6 WREG: Write Registers

The WREG command is a two-byte opcode followed by the input of the register data. The first byte contains the

command opcode and the register address. The second byte of the opcode specifies the number of registers to write – 1.
First opcode byte: 010r rrrr, where r rrrr is the starting register address.
Second opcode byte: 000n nnnn, where n nnnn is the number of registers to write – 1.
After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 5. The WREG command can be issued at any time.

7.6.7 SPI Reset

The device has a Power-On Reset (POR) circuit block, which will reset the SPI interface after powering on, in <100 ms. The SPI interface can also be reseted by asserting RESET.
Once reseted, both the SPI transfer state and the internal registers will be assigned to its default values.
Because the CN121 SPI transfer state and the internal registers will not be cleared between each SPI transaction, it is **strongly required** RESET must be connected to MCU GPIO and used every time the system initializes.

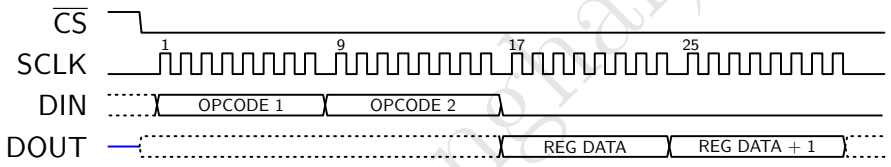


Figure 4: RREG command example: read two registers starting from register 00h (OPCODE1=0010 0000, OPCODE2=0000 0001)

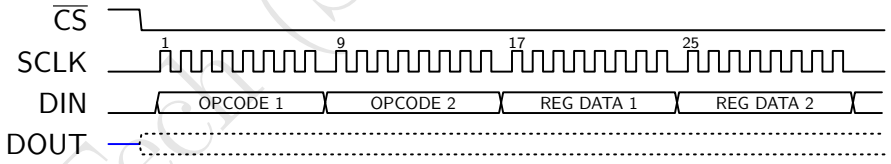


Figure 5: WREG command example: write two registers starting from register 00h (OPCODE1=0100 0000, OPCODE2=0000 0001)

8 Register Definition

Table 6: Register assignments

ADDRESS	REGISTER	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	CONFIG	00h	N/A	PD	STANDBY	N/A	N/A	N/A	N/A	N/A
01h	CH_SET	00h	CH_FR	CH_HP	CH_LP[1]	CH_LP[0]	CH_GAIN[3]	CH_GAIN[2]	CH_GAIN[1]	CH_GAIN[0]

8.1 CONFIG: Configuration Register (address = 00h)

This register configures the power mode of the device.

Table 7: CONFIG: configuration register field descriptions

Bit 7	Not Applicable
Bit 6	PD: Chip power-down
	This bit powers down the chip, and has a higher priority over the STANDBY bit. 0 = the chip leaves the shut-down mode (default) 1 = the chip enters the shut-down mode
Bit 5	STANDBY: Chip standby mode
	This bit makes the chip work in standby mode, owns a lower priority than the PD bit. 0 = the chip enters the sensing mode (default) 1 = the chip enters the standby mode
Bits[4:0]	Not Applicable

8.2 CH_SET: Channel Set Register (address = 01h)

This register sets the ECG channel in the sensing mode.

Table 8: CH_SET: channel set register field descriptions

Bit 7	CH_FR: Channel Fast Restore
	This bit enables the fast restore mode of the channel, and has the highest priority. 0 = fast restore disabled (default) 1 = fast restore enabled
Bit 6	CH_HP: Channel High-pass Pole
	This bit selects the high-pass pole for the channel. 0 = 4Hz (default) 1 = 0.05Hz
Bits[5:4]	CH_LP[1:0]: Channel Low-pass Pole
	These bits select the low-pass pole for the channel. 00 = 40Hz (default) 01 = 55Hz 10 = 150Hz 11 = 300Hz
Bits[3:0]	CH_GAIN[3:0]: Channel Gain
	These bits select the gain of the channel. 0000 = 60 (default) 0001 = 120 0010 = 180 0011 = 240 0100 = 300 0101 = 360 0110 = 420 0111 = 480 1000 = 540 1001 = 600 1010 = 660 1011 = 720 1100 = 780 1101 = 840 1110 = 900 1111 = 960

9 Application Information

NOTE

Information in this section is not part of the CyzurTech component specification, and CyzurTech does not warrant its accuracy or completeness. CyzurTech customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application Circuit

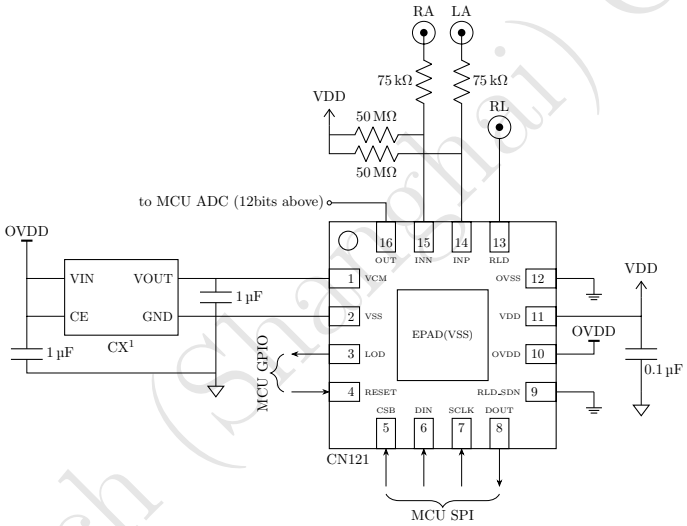


Figure 6: Typical application circuit (3 electrodes configuration)

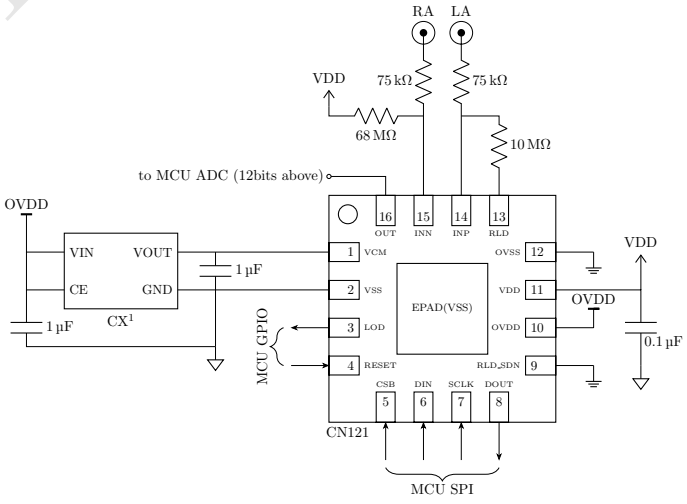


Figure 7: Typical application circuit (2 electrodes configuration)

[1]customized 0.9V LDO chip

10 Package Outline Drawing

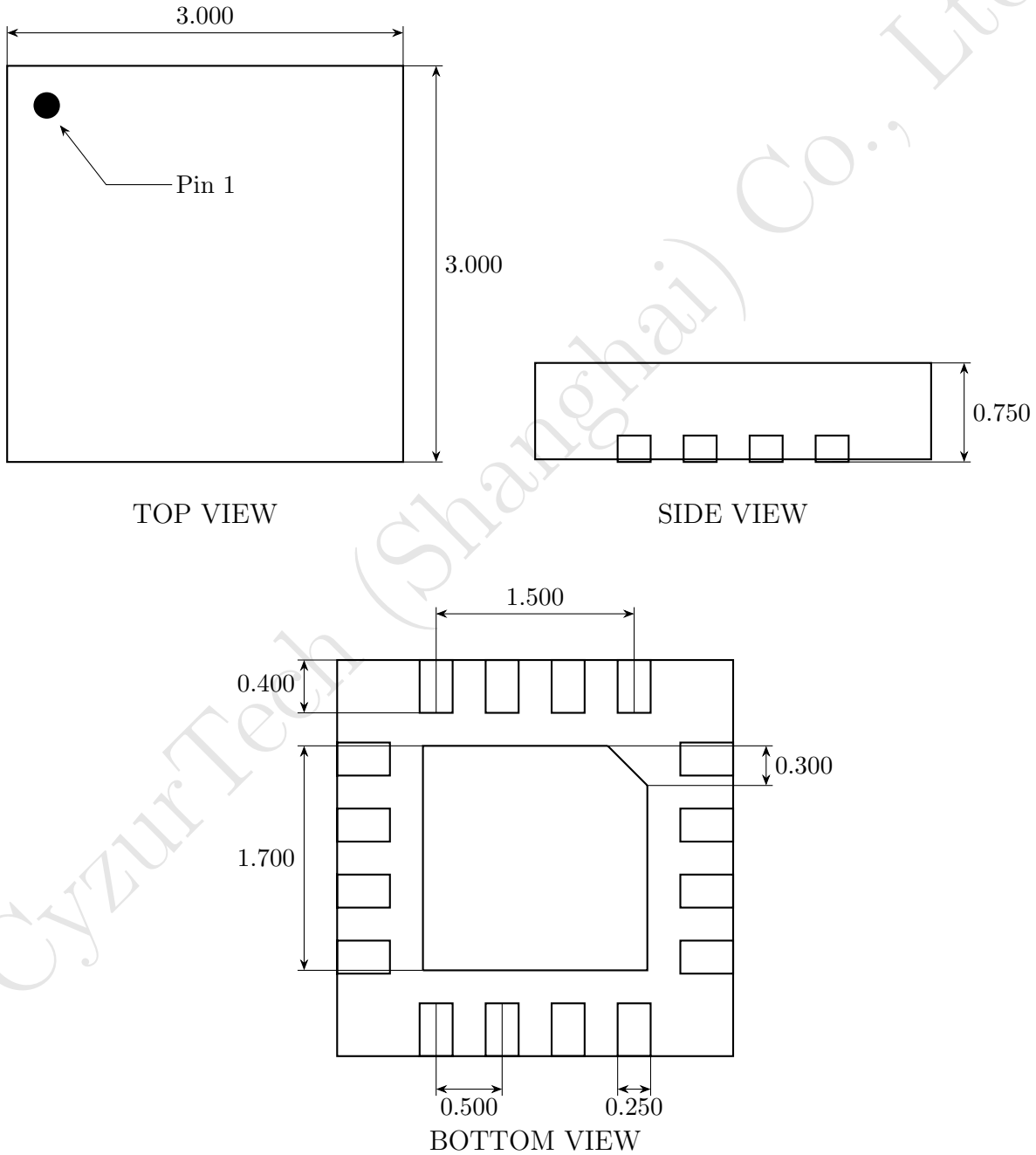
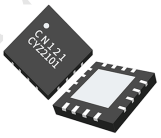
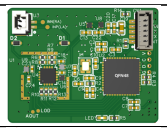


Figure 8: 16-Pin Quad Flat No-Lead Package (QFN16)
Dimensions shown in millimeters

11 Ordering Guide

Device	Type	Description	Package	Picture
CN121	Chip	1-channel analog front-end chip.	QFN16 3 × 3 mm	
CNM7000-2	Module	Hand-held cardiac activity monitoring module with 2 electrodes (clinical level)	PCBA 30mm×23mm×5.6mm	
CNM7000-3	Module	Hand-held cardiac activity monitoring module with 3 electrodes (clinical level)	PCBA 30mm×23mm×5.6mm